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09/741,634	12/19/2000	John G. Sikonia	595.03-US1	5633

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SANDRA P. THOMPSON
RUTAN & TUCKER, LLP
611 ANTON BLVD.
14TH FLOOR
COSTA MESA, CA 92626-1998

EXAMINER	
ROCHE, LEANNA M	
ART UNIT	PAPER NUMBER
1771	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/741,634	SIKONIA, JOHN G.
	Examiner	Art Unit
	Leanna Roche	1771

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8,10-15 and 17-34* is/are pending in the application.

4a) Of the above claim(s) *18-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8,10-15,17 and 34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 18-33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group II, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

In view of the amendment filed in Paper No. 7, the election of species requirement set forth in Paper No. 4 is withdrawn, and all pending claims from Group I, Claims 1-5, 8, 10-15, 17 and 34, have been fully examined.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference numbers 126 and 146 are not shown in any of Figures 1-4. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 5, 8, 15, 17 and 34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 is dependent upon Claim 3 which is dependent on Claim 1. Claim 3 teaches that the first layer comprises a nanoporous material. Claim 1 teaches that the second layer is nanoporous. Therefore, Claim 8 is considered vague and indefinite because it unclear if the nanoporous material comprised of a polymer, taught in Claim 8, refers to material of the first layer as described in Claim 3, the material of the second layer as described in Claim 1, or the materials of both the first and second layers. Clarification is required. For the purposes of examination, the examiner has read Claim 8 to mean, "a first layer comprised of a nanoporous polymer having a second layer which is also nanoporous but may be comprised of any material".

Claim 15 teaches a layer of metal wire between the substrate and the first layer. However, Claim 1, on which Claim 15 depends, teaches that the first layer is juxtaposing a substrate. The definition of the term juxtapose is "to place side by side" (Merriam-Webster's Collegiate Dictionary, 10th edition). It is unclear how a layer of metal wire may be placed between the substrate layer and the first layer, if the substrate layer and the first layer are specified as being side by side. Clarification is required. For the purposes of examination, the examiner has interpreted this limitation to mean that a metal layer may be partially placed between the first layer and the substrate layer, such that the first layer and substrate layer still have at least a partial interface between.

Claim 34 is dependent upon Claim 3 which is dependent on Claim 1. Claim 3 teaches that the first layer comprises a nanoporous material. Claim 1 teaches that the second layer is nanoporous. Therefore, Claim 34 is considered vague and indefinite because it unclear if the nanoporous material comprised of an adamantane-based compound, as taught in Claim 34, refers to material of the first layer as described in Claim 3, the material of the second layer as described in Claim 1, or the materials of both the first and second layers. Clarification is required. For the purposes of examination, the examiner has read Claim 34 to mean, "a first layer comprised of an adamantane-based compound having a second layer which is also nanoporous but may be comprised of any material".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8, 10-15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USPN 5858869) in view of O'Neill et al. (USPN 6187248).

Chen teaches a method for fabricating intermetal dielectric insulation layers in integrated circuits on semiconductor substrates. Chen discloses a substrate layer (10) having a silicon oxide layer (12) disposed thereon. A silicon oxide liner layer (18) is

disposed on silicon oxide layer (12), and a low dielectric constant polymer layer (20), which may be comprised of an organic material such as a polyimide, is disposed on the silicon oxide liner layer (18) of Chen (See Figure 3, and Column 2, lines 38-48). The substrate layer (10) of Chen reads on Applicant's substrate layer. The silicon oxide layer (12) of Chen reads on Applicant's first layer juxtaposing a substrate. The silicon oxide liner layer (18) of Chen reads on Applicant's second layer juxtaposing the first layer. The low dielectric constant polymer layer (20) of Chen reads on Applicant's additional layer partially juxtaposing the second layer and also reads on Applicant's additional layer comprising an organic compound.

Chen does not specifically teach that their second layer is nanoporous, specifically a nanoporous material having a mean void diameter of less than 100 nanometers (Claim 14). O'Neill, however, teaches that it is well known in the art of integrated circuits that the incorporation of porosity into polymeric materials reduces the dielectric constant of the polymeric material (Column 1, lines 41-42). O'Neill also teaches nanoporous polyarylene ether films that may be used in place of the traditionally used silicon oxide and polyimide nanofoam interlayer dielectric materials of integrated circuits. The nanoporous polyarylene ether films of O'Neill have dielectric constant values of less than 2.0, and display improved adhesion for use in dielectric layers for integrated circuits. The nanoporous polyarylene ether films of O'Neill also have an average pore size of less than 30 nanometers. Therefore, it would have been obvious to the skilled artisan at the time this invention was made to substitute the nanoporous polyarylene ether films of O'Neill for the silicon oxide liner layer (18) of

Chen, motivated by the desire to produce an integrated circuit with increased overall performance and improved adhesion due to the nanoporous nature of the material and the reduction in the dielectric constant of the interlayer dielectric material.

With regard to Claim 2, Chen does not specifically disclose a dielectric constant of no more than 2.5. However, Chen states that it is very desirable to minimize the dielectric constant in the insulator material between the conducting lines of an integrated circuit to increase the performance of the overall circuit (Column 1, lines 8-58). Therefore, it would have been obvious to the skilled artisan at the time this invention was made to minimize the dielectric constant of the intermetal dielectric material of Chen, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. See *In re Aller*, 105 USPQ 233. In the present case, it would have been obvious to use an intermetal dielectric material having a dielectric constant less than 2.5 to improve the overall performance of the integrated circuit.

Chen does not specifically disclose that their first layer may be nanoporous (Claims 3-5 and 8). O'Neill, however, teaches that it is well known in the art of integrated circuits that the incorporation of porosity into polymeric materials reduces the dielectric constant of the polymeric material (Column 1, lines 41-42). O'Neill also teaches nanoporous polyarylene ether films that may be used in place of the traditionally used silicon oxide and polyimide nanofoam interlayer dielectric materials of integrated circuits. The nanoporous polyarylene ether films of O'Neill have dielectric constant values of less than 2.0, and display improved adhesion for use in dielectric

layers for integrated circuits. Therefore, it would have been obvious to the skilled artisan at the time this invention was made to substitute the nanoporous polyarylene ether films of O'Neill for the silicon oxide layer (12) of Chen, motivated by the desire to produce an integrated circuit with increased overall performance and improved adhesion due to the nanoporous nature of the material and the reduction in the dielectric constant of the interlayer dielectric material.

Chen does not specifically disclose that their first layer is comprised of an organic polymer (Claims 4 and 8) such as polyarylene ether (Claim 5). O'Neill teaches nanoporous polyarylene ether films that may be used in place of the traditionally used silicon oxide and polyimide nanofoam interlayer dielectric materials of integrated circuits because they have dielectric constant values of less than 2.0, and display improved adhesion for use in dielectric layers for integrated circuits. Therefore, it would have been obvious to the skilled artisan at the time this invention was made to substitute the nanoporous polyarylene ether films of O'Neill for the silicon oxide layer (12) of Chen, motivated by the desire to produce an integrated circuit with increased overall performance and improved adhesion due to the nanoporous nature of the material and the reduction in the dielectric constant of the interlayer dielectric material.

Chen does not specifically disclose that their second layer is comprised of a nanoporous polymer (Claim 10) such as polyarylene ether (Claim 11). O'Neill, however, teaches that it is well known in the art of integrated circuits that the incorporation of porosity into polymeric materials reduces the dielectric constant of the polymeric material (Column 1, lines 41-42). O'Neill also teaches nanoporous polyarylene ether

films that may be used in place of the traditionally used silicon oxide and polyimide nanofoam interlayer dielectric materials of integrated circuits. The nanoporous polyarylene ether films of O'Neill have dielectric constant values of less than 2.0, and display improved adhesion for use in dielectric layers for integrated circuits. Therefore, it would have been obvious to the skilled artisan at the time this invention was made to substitute the nanoporous polyarylene ether films of O'Neill for the silicon oxide liner layer (18) of Chen, motivated by the desire to produce an integrated circuit with increased overall performance and improved adhesion due to the nanoporous nature of the material and the reduction in the dielectric constant of the interlayer dielectric material.

With regard to Claims 12 and 13, Chen discloses a low dielectric constant polymer layer (20) comprised of an organic material such as polyimide, but does not disclose that their low dielectric constant polymer layer (20) is comprised of a polyarylene ether compound. O'Neill teaches nanoporous polyarylene ether films that may be used in place of the traditionally used silicon oxide and polyimide interlayer dielectric materials of integrated circuits because they have dielectric constant values of less than 2.0, and display improved adhesion for use in dielectric layers for integrated circuits. Therefore, it would have been obvious to the skilled artisan at the time this invention was made to substitute the nanoporous polyarylene ether films of O'Neill for the low dielectric constant polymer layer (20) of Chen, motivated by the desire to produce an integrated circuit with increased overall performance and improved

adhesion due to the nanoporous nature of the material and the reduction in the dielectric constant of the interlayer dielectric material.

With regard to Claims 15 and 17, Chen teaches a silicon oxide liner layer (18) disposed on silicon oxide layer (12). A low dielectric constant polymer layer (20) is disposed on the silicon oxide liner layer (18) of Chen. A hard mask layer (22) comprised of a fluorine doped silicon oxide is disposed on the low dielectric constant polymer layer (20) (See Figure 3, and Column 2, lines 38-48). In this instance, the silicon oxide layer (12) of Chen reads on Applicant's substrate. The silicon oxide liner layer (18) of Chen reads on Applicant's first layer. The low dielectric constant polymer layer (20) of Chen reads on Applicant's second layer. The hard mask layer (22) of Chen reads on Applicant's additional layer. Chen also teaches metal lines (16), which may be comprised of aluminum or copper, between silicon oxide liner layer (18) and silicon oxide layer (12). This reads on Applicant's metal wire of either aluminum or copper between the substrate and the first layer.

Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (USPN 5858869) in view of O'Neill et al. (USPN 6187248) as applied to Claims 1 and 3 above, and further in view of Lau et al. (USPN 6509415).

Neither Chen nor O'Neill disclose a first and/or second layer comprised of a nanoporous adamantane-based compound. Lau, however, teaches that in order to accommodate the decreasing size of the functional elements of integrated circuits, materials having dielectric constants of less than 3.0 are needed immediately. Lau also

states that there is a strong need for dielectric materials containing nanoporosity, and Lau teaches that their low dielectric constant material avoids the problems of previous nanoporous dielectric materials such as poor distribution of the nanopore producing material (glass sphere or fullerene), poor control over pore size, and/or a tendency to collapse. Lau is directed to the use of low dielectric constant organic dielectrics based on cage-like structures for use as insulator materials in integrated circuits. The low dielectric constant materials of Lau are nanoporous and incorporate adamantane as the cage-like structures forming the nanopores (Column 1 line 50 - Column 2 line 62). Therefore, it would have been obvious to the skilled artisan at the time this invention was made to combine the teachings of Chen and Lau by substituting the low dielectric material of Lau for the intermetal dielectric material of Chen in view of O'Neill, motivated by the desire to produce an integrated circuit which will perform efficiently despite any decreased size of functional elements, which is displays good pore size and distribution, and which is not susceptible to collapse.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Low et al. (USPN 3694700) discloses the basic structure of an integrated circuit chip. Kondo et al. (USPN 5635301) was cited in Applicant's specification. Burgoyne, Jr. et al. (USPN 5658994) teaches the use of polyarylene ether polymers as low dielectric materials for insulating layers of integrated circuits. Jeng et al. (USPN 5818111) discloses an integrated circuit comprised of layers of low

dielectric material alternating with stabilizing materials. Yang et al. (USPN 6162583) teaches an integrated circuit comprising three intermetal dielectric layers disposed on an insulation layer.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leanna Roche whose telephone number is 703-308-6549. The examiner can normally be reached on Monday through Friday from 8:30 am to 6:00 pm (with alternate Mondays off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Terrel Morris can be reached on 703-308-2414. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

lmr
January 24, 2003

TERREL MORRIS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700